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A Comprehensive Simulation Model for Floating Gate Transistors

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by

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Abstract

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Floating-gate transistors have proven to be extremely useful devices in the development of analog systems; however, the inability to properly simulate these devices has held back their adoption. The objective of this work was to develop a complete simulation model for a floating-gate (FG) MOSFET using both standard SPICE primitives and also MOSFET models taken directly from foundry characterizations. This new simulation model will give analog designers the ability simulate all aspects of floating-gate device operation including transient, AC and DC characteristics. This work describes the development of this model and demonstrates its use in various applications.

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Chapter 1

Introduction

In today's increasingly mobile world, we are demanding more computational capacity than ever before and expect it to be available anytime in the palm of our hands. Integrated-circuit processes are reducing power requirements, and advancements in battery technology are being made; however, low-power analog systems still require orders of magnitude less power than comparable digital systems. Analog and mixed-signal systems offer tremendous computational capacity at very little cost in terms of power.

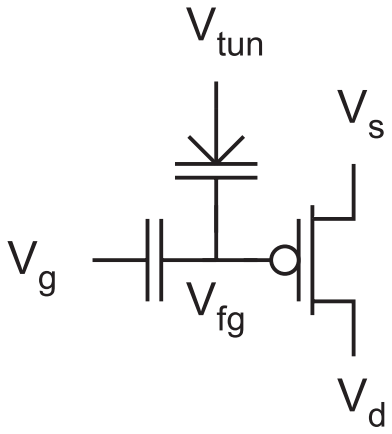


Figure 1.1: Schematic of a typical floating gate transistor.

One major weakness in analog integrated circuits is inaccuracies in the manufacturing process, which is manifested in device mismatch. Because analog systems depend greatly on specific currents flowing through various devices, overall system performance can be

significantly degraded if devices are not fabricated to their designed specifications. Floating-gate transistors, because of their programmability, are an effective solution to this problem. A floating-gate transistor, seen in Figure 1.1, is a standard CMOS Field Effect Transistor (FET) with only capacitive connections to the gate [1] (V_{fg} in Figure 1.1). With no DC path to ground, a charge can be stored on this gate which will affect the current through the device for a given bias applied to the control gate. This ability to store an initial charge on the floating gate allows fabrication imperfections to be corrected for devices that are required to be precisely matched, such as the input transistors of a differential pair or a current mirror.

The ability to alter the charge during operation on a floating gate transistor also allows for adaptation and learning systems to be developed with relative ease [2][3]; furthermore, this feature also provides the analog designer with an analog memory element [4]. Analog memory is well suited for very large systems; moreover, you can use floating-gate devices for switch elements, similar to SRAM. This memory element is a key component in reconfigurable systems like the Field Programmable Analog Array (FPAA). These FPAAs are the analog counterpart to the Field Programmable Gate Arrays (FPGA) found in the digital realm and are described in [5][6].

There are many uses of the floating gate transistor, but there is one glaring flaw: there currently exists no simulation model for this very useful element. Because there is no DC path to ground from the floating gate of the transistor, standard simulators are unable to converge on a DC solution and, therefore, cannot simulate the device. Also, the two quantum mechanical processes used to alter the charge on the floating gate are not directly modeled in SPICE (Simulation Program with Integrated Circuit Emphasis) simulators.

There currently exists no way to design systems using floating-gate transistors because no complete simulation model exists. Without a simulation model for these devices, the only way to test a design is to have it fabricated. Currently, the engineer will design a circuit in which floating gates are required and simulate as much as possible, usually by replacing a floating-gate transistor in the circuit with a standard MOSFET. Once this designed circuit is performing to the specifications, the floating-gate transistors are put into the system and the chip is fabricated without simmulating the effects of the floating-gate transistors on the system. This process is repeated until a chip is returned which performs to the designed

specifications. This design process is extremely time-consuming because the average turn-around time for a fabrication run is three months. Fabricating a chip is also an expensive endeavor and thus drives up the cost of designing with floating-gate transistors and ultimately the final shipping product.

The objective of this research was to develop a complete simulation model for a floating-gate (FG) MOSFET using both standard SPICE primitives and also MOSFET models taken directly from foundry characterizations. Using standard SPICE primitives will allow the proposed model to be used with all industry standard simulators, such as Spectre by Cadence and various SPICE programs (i.e. HSPICE, WinSPICE, etc), with no changes to the circuit and minimal changes to the code to comply with the specific simulator's syntax. The creation of this model will allow analog designers to create circuits using floating-gate transistors faster and cheaper than ever before by giving the engineer the ability to simulate the entire system accounting for the various differences between standard CMOS FETs and floating-gate FETs.

This document describes our resulting model and its implementation; Chapter 2 describes in detail the floating gate transistor and previous efforts to model its behavior, Chapter 3 shows our proposed model and Chapter 4 demonstrates the effectiveness of this proposed model.

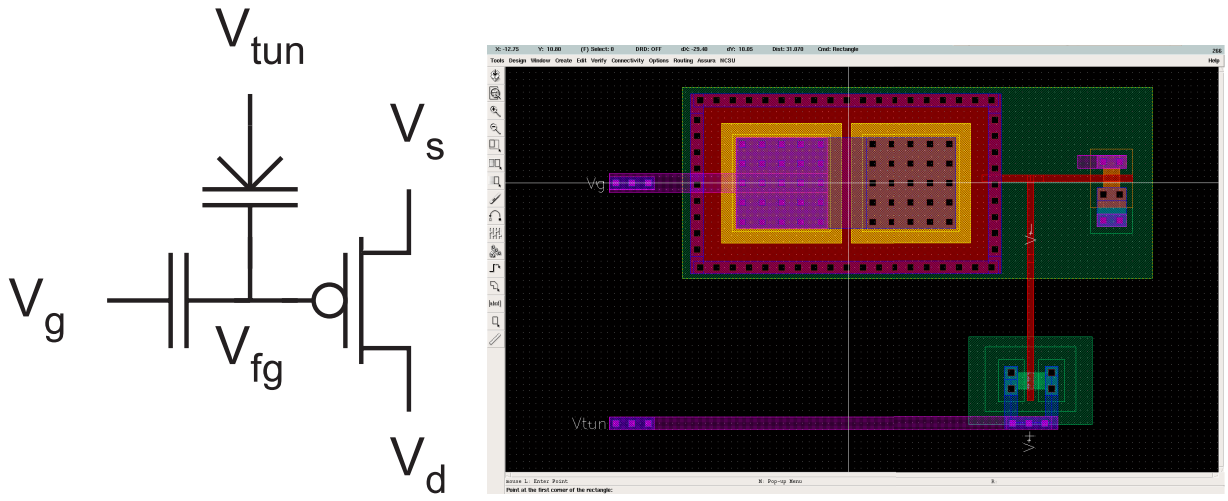
Chapter 2

Floating-Gate Transistors

Floating-gate transistors are extremely similar to standard CMOS FETs, but do differ in several critical ways. In this chapter we discuss the floating-gate transistor in detail, covering specifically how it differs from a standard CMOS FET. To build a comprehensive simulation model, we must account for 2 characteristics of floating-gate transistors: (1) programming using two quantum mechanical processes discussed in Sections 2.4 and 2.3, and (2) DC characteristics discussed in Section 2.2. Section 2.1 details how a floating-gate transistor is fabricated using standard CMOS processes, and Section 2.5 discusses previous efforts to model floating-gate transistors in section of this chapter.

2.1 Fabrication of Floating-Gate Transistors

Floating-gate transistors are fabricated using a standard CMOS p-channel FET (referred to in this document as a pFET) with a capacitor and a tunneling junction connected to the gate of the pFET. These elements electrically isolate the gate of the transistor allowing for charge storage and resulting in various changes in operational characteristics such as a reduction in effective output resistance and coupling from each terminal onto the floating gate (including multiple-input floating gates). Hot-electron injection is more easily control in pFETs than in nFETs and as a result pFETs are most often used to create floating-gate devices. Seen in Figure 2.1, connected directly to the polysilicon gate of the pFET are a tunneling junction, used for removing electrons from the floating gate, and a standard



(a) (b)

Figure 2.1: a)Schematic of a typical floating gate transistor. The arrow on C_{tun} shows that this capacitor is not a standard parallel plate capacitor but a tunneling junction fabricated using a MOSCap or varactor. b)Layout drawing of a typical floating-gate transistor drawn using Virtuoso Layout Editor. The dominant element seen is the capacitor through which the control gate is coupled to the floating gate, on the right is the MOSFET device and in the lower right is the tunneling junction. It is to be noted that there is no direct connection to the gate of the MOSFET and the connections of the input capacitor and tunneling junction are made using a layer of polysilicon.

parallel-plate capacitor, through which the control gate is coupled.

The tunneling junction is typically made from one of two devices: (1) MOS Capacitor (MOSCap) or (2) Varactor. The MOSCap is fabricated using a standard MOSFET, connecting the drain, source and well of the device to the tunneling potential (V_{tun}) and the gate of the device to the floating node of the floating-gate transistor.

2.2 DC Characteristics

Electrically isolating the gate of a MOSFET, such as is done in a floating-gate MOSFET, results in several changes to key DC characteristics. Each terminal on the device is coupled to the floating gate through parasitic capacitances and this coupling affects the DC response of the device. The capacitive coupling of the terminals of the transistor will cause changes in the channel current. Because the gate of the transistor is not "pinned" to a voltage, as

the potential of the other terminals are changed the potential on the gate will also change in accordance with some coupling coefficient determined by the size of the capacitor with respect to the total capacitance on the floating node. This change in the potential on the gate will then alter the channel current in accordance with the equations which govern typical MOSFET operation. The charge on the floating gate is described by

$$V_{fg} = \frac{Q}{C_T} + \sum \frac{C_i}{C_T} V_i \tag{2.1}$$

where C_i is the capacitance seen between the floating gate and the given terminal (i.e. drain, source, well), C_T is the total capacitance on the floating gate, V_i is the voltage on the given terminal, and Q is the charge stored on the floating gate. Specifically, the coupling of the drain back to the floating gate alters the effective Early voltage, and in cases where the input capacitor is comparable to the parasitic capacitances, the result is an exponential response in the saturation region of operation when the transistor is operating in subthreshold. This additional parasitic coupling also adds to the capacitance seen across the oxide which alters the constant, κ, which reflects this capacitance.

2.3 Hot-Electron Injection

Hot-electron injection is the process by which electrons are added to the gate of a MOSFET transistor. In a standard MOSFET, this effect is considered to be a non-ideality in the device. Hot-electron injection creates a current flowing between the gate and channel of the transistor in defiance of the operational model of MOSFETs. This effect, used in conjunction with the Fowler-Nordheim tunneling process discussed previously, gives the ability to precisely control the charge on the floating gate. For this injection to take place, two conditions must be met: (1) there must be current flowing through the channel of the transistor and (2) there must be a large electric field between the gate and drain. The large electric field between the gate and drain is typically created by raising the potential difference between the source and drain. If both of these conditions are met, carriers flowing through the channel will be energized enough to impact-ionize an electron-hole pair at the drain end of the channel. The large gate-to-drain potential will then cause some electrons to move in the

direction of the gate with enough energy to cross the oxide barrier to the gate where they are held by the floating nature of that node. These added electrons on the gate can be observed as a change in the threshold voltage of the floating-gate transistor, and an increase in current for a given bias condition. Figure 2.2 clearly shows the decrease in threshold voltage with respect to V_{dd} and higher current levels resulting from this process.

2.4 Fowler-Nordheim Tunneling

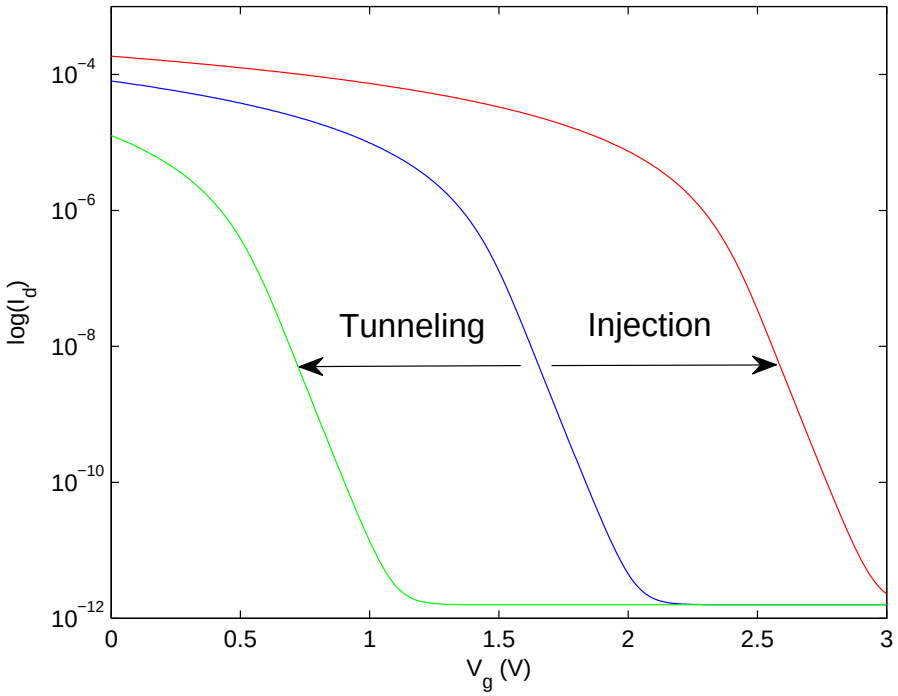
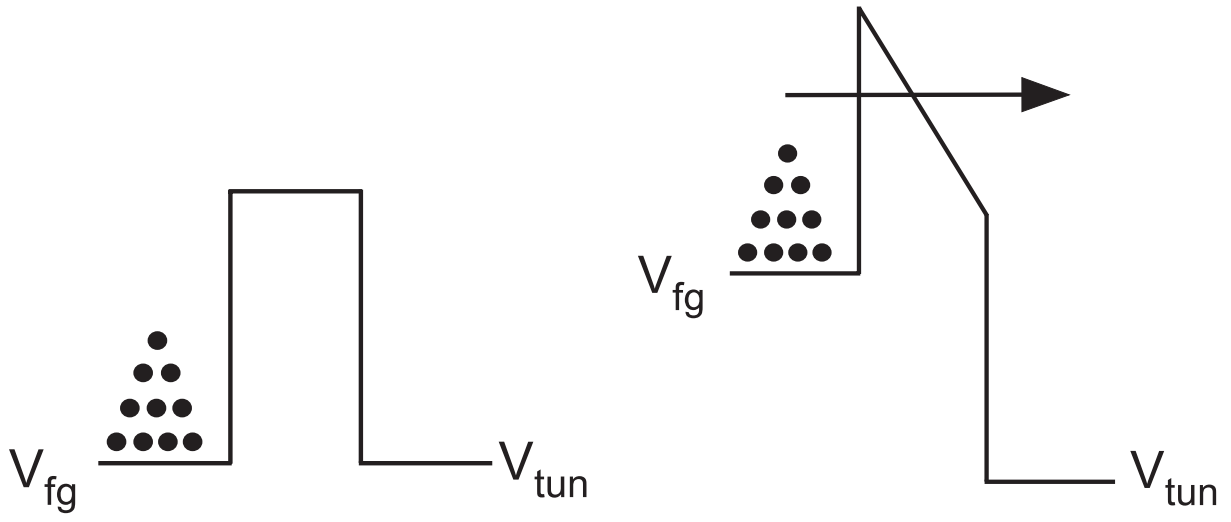


Figure 2.2: Gate sweeps showing the effects of Hot-electron injection and Fowler-Nordheim tunneling. The middle trace is a sweep taken prior to either process being performed, the left trace demonstrates the effect of Fowler-Nordheim tunneling on the threshold voltage and current levels, and the right trace demonstrates the effect of Hot-electron injection on the threshold voltage and current levels.

Fowler-Nordheim tunneling is the quantum mechanical process used to remove electrons from an isolated floating node in a circuit. This process is used to remove electrons from the floating gate of the transistor and raise the effective threshold voltage of the device with respect to V_{dd}. Charge is held on the floating gate using an insulator, typically silicon dioxide



(a) (b)

Figure 2.3: a)Tunneling junction with no potential difference across the insulator. b)Tunneling junction with a high potential difference across the insulator allowing electrons to tunnel through the insulator's barrier.

(SO_2). This insulator acts as a barrier to the transport of electrons because an electron must rise to an energy level above that of the insulator, approximately 3.02eV, to overcome this barrier. To tunnel electrons through this barrier, we raise the potential difference across the insulator which effectively reduces the thickness of the insulating oxide. This reduction in thickness, as depicted in Figure 2.3, creates an area through which some electrons will have the energy to "jump through" without degrading the insulator. As electrons are tunneled off the floating gate, the overall charge on the gate becomes more positive and increases the effective threshold voltage of the transistor with respect to V_{dd}. This increase in effective threshold voltage produces a corresponding reduction in current flowing through the device for a given bias condition, as can be seen in Figure 2.2.

2.5 Previous Modeling Attempts

There have been several attempts at modeling floating-gate transistors in the past, but because of the difficulties in modeling floating-gate devices these models have been simplistic and very limited. There are some structures that have become popular within the analog de-

signer community. The most popular modeling structures are a "coupling" model developed by Mondragon-Torres et al.[7] and a synapse model shown by Rahimi et al.[8] and Gray et al.[9]. The coupling model in [10] focuses mainly on modeling how the parasitic capacitances effect the operational characteristics of the device. The synaptic models shown in [8] and [9] concentrate on the charge alteration aspect of floating-gate transistor operation creating models that work well in adaptive applications and pulse-based applications respectively. These structures each have their own strengths, but all of them have significant limitations which are discussed in detail in the following sections.

2.5.1 Coupling Model

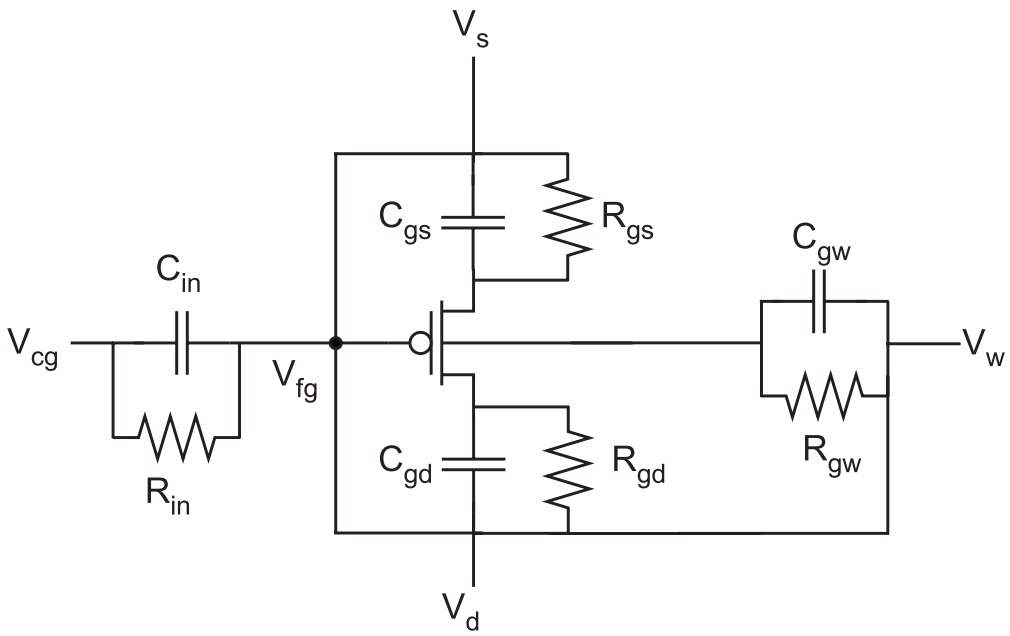


Figure 2.4: Schematic of the Floating-Gate MOSFET model proposed by Sanchez-Sinencio et al. DC convergence is achieved by placing a large valued resistor in parallel with each drawn capacitor connecting to the floating node. The reduced output capacitance caused by coupling through parasitic capacitors is modeled by explicitly drawn capacitors of comparable size.

As seen in Figure 2.4 the structure presented by Sanchez-Sinencio et al.[10] models the effect of parasitic capacitors as well as the coupling effect of the input capacitor by explicitly drawing all these capacitors on the schematic. V_{cg} is the control gate voltage, V_{fg} is the

voltage on the floating node, V_s is the source voltage, V_d is the drain voltage and V_w is the well potential. To address the issue of DC convergence a large resistor is connected in parallel with each capacitor. These resistors also allow each terminal to contribute to the charge seen by the floating gate during a DC simulation. These resistors are selected such that they are sufficiently large to be neglected in the AC case; moreover, the size of the resistors are also selected such that the RC product of each resistor-capacitor pair is equal [10]. The sizing of these resistors are further discussed in Appendix A.

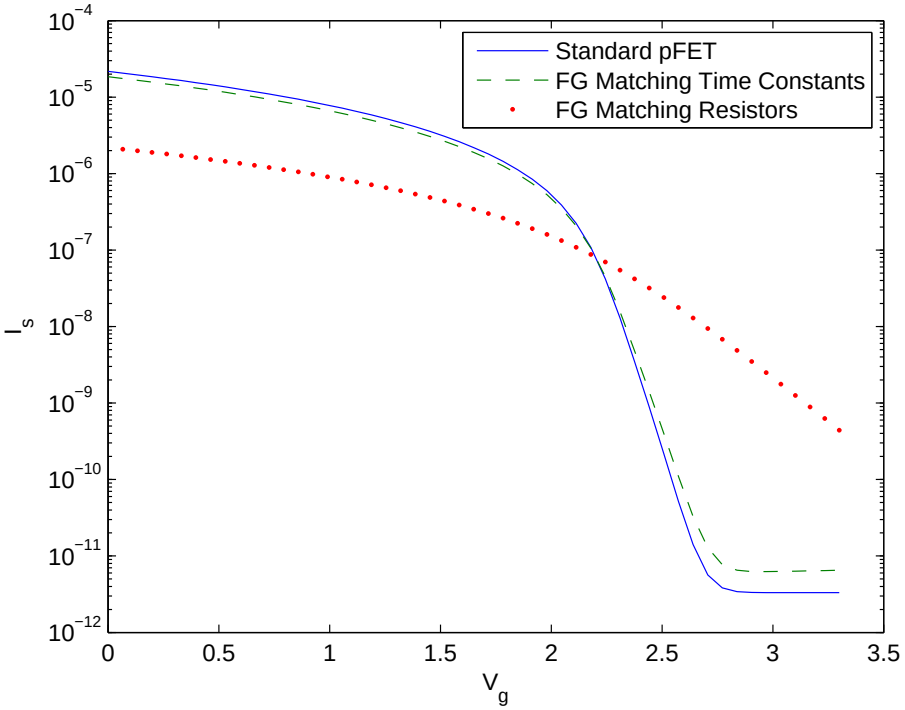


Figure 2.5: Gate sweeps of Sanchez-Sinencio et al's Floating-Gate MOSFET with matching time constants (dashed line), Sanchez-Sinencio et al's Floating-Gate MOSFET with matching resistors (dotted line) and an equally sized standard MOSFET (solid line).

One of the key observable effects of coupling the control gate voltage, V_{cg}, through an input capacitor and leaving the physical gate of the transistor floating is a change in the slope constant κ as described in Section 2.2. Figure 2.5 shows this change in κ very clearly. The other key effect of leaving the physical gate of the transistor floating is a result of the coupling of a gate-to-drain capacitance and gate-to-source capacitance. This effect is apparent when sweeping the drain potential and observing the channel current; the output

resistance of a typical floating-gate device will be lower than that of a standard MOSFET and is reflected in the slope of the saturation region of the drain sweep curves. Figure 2.6 shows the drain sweep curves for a standard MOSFET, a floating-gate MOSFET and the model proposed by Sanchez-Sinencio et al in [10] and [7]; furthermore, it can be seen in this figure that the proposed model shows a reduction in output resistance that is expected for floating-gate devices.

Sanchez-Sinencio et al.[11] also introduce a modification to this model where an independent voltage source is connected to the floating gate to apply an initial charge to the gate. This charge, however, cannot be altered. An additional modification is shown in [7] where a series of dependent voltage sources are connected through a resistor to the floating gate to apply charge coupling from the various terminals of the device rather than explicitly drawing a resistor-capacitor pair for each. The series of voltage-controlled voltage sources connected to the gate allows the effects of the capacitive coupling from other terminals to be modeled.

Overall, this model and its variants are very limited because they lack an implementation of Hot-electron injection and Fowler-Nordheim tunneling. This model could be used to test the DC and AC responses of a system that is not using any programming functionality during normal operation (i.e. Hot-electron injection and Fowler-Nordheim tunneling are used to program an initial operating point for the system). This model is also useful for modeling the operation of multiple input floating-gate transistors (MIFG); however, it is still impossible to simulate adaptive systems using this model. This model is useful in evaluating the performance of a multiple input floating-gate transistor (MIFG). Additional inputs are easily added to the model simply by adding additional connections to the floating node through a resistor-capacitor pair.

2.5.2 Synaptic Model

In [8], Rahimi et al propose a simulation structure that remedies many of the short comings of the coupling model proposed by [10] and [7] in Section 2.5.1. Specifically, Rahimi et al focus on modeling Hot-Electron Injection and Fowler-Nordheim Tunneling in a manner suitable for use in adaptive systems [12][13]. The devices used in these adaptive systems

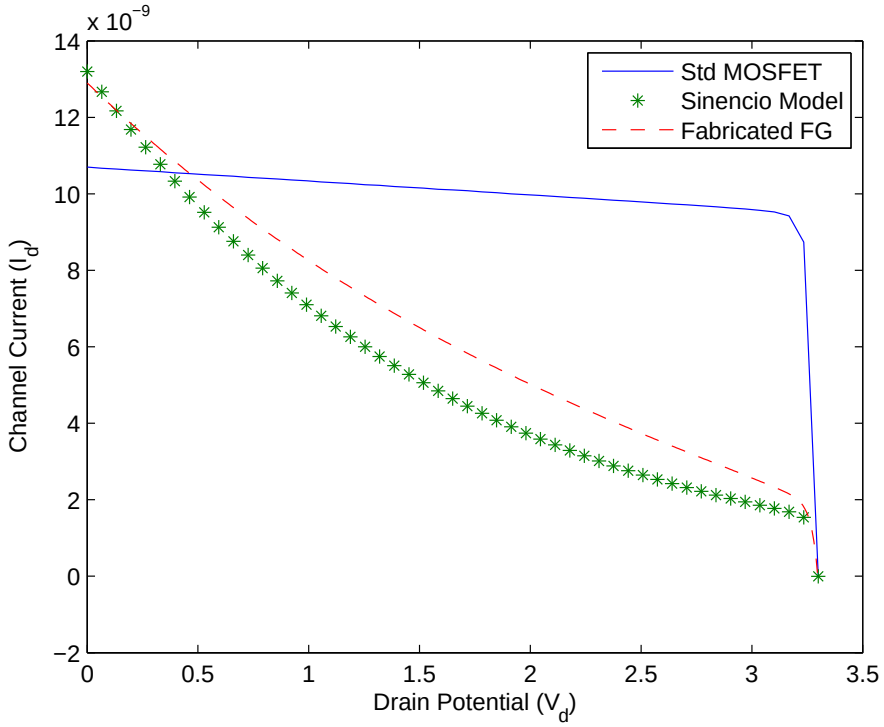


Figure 2.6: Drain sweep curves for a standard MOSFET, a fabricated floating-gate transistor and the model developed by Sanchez-Sinencio et al. The reduction in output resistance is clearly visible in the floating-gate data and Sanchez-Sinencio et al's model handles this reduction in output resistance well.

are often referred to as "synapses" because their behavior in many ways is similar to the biological synapses of neurons.

Three currents are modeled in this structure: the current flowing from the tunneling junction to the floating node, the injection current flowing from the channel to the floating node and a well current flowing from the channel to the well of the device. These currents are modeled by three voltage-controlled current sources as shown in Figure 2.7. These elements are controlled by empirical equations fit from data using directly measurable voltages and currents through exposed terminals.

The current produced through Fowler-Nordheim Tunneling is well understood [14] and depends on the voltage across the oxide and the width, length and thickness of the oxide. This current and its dependencies are described by:

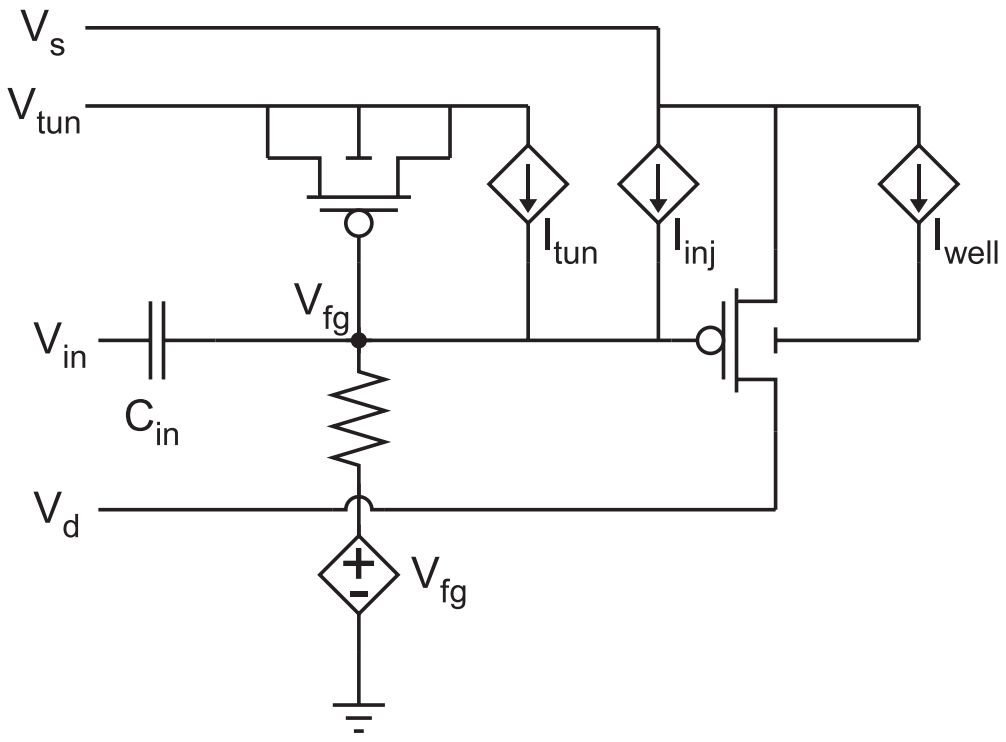
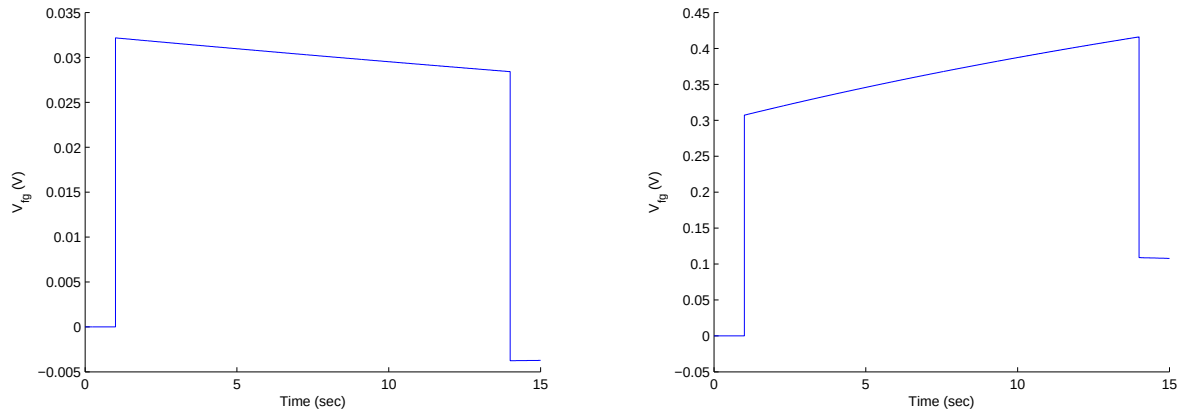


Figure 2.7: Schematic of the Floating-Gate MOSFET model proposed by Rahimi et al. DC convergence is achieved in the same manner as in [10] by placing a large-valued resistor between the floating node and a DC voltage source configured such that no current flows through the resistor. Hot-Electron Injection and Fowler-Nordheim Tunneling are modeled by voltage controlled voltage sources whose characterisitics are defined by empirical equations governing the two processes.

$$I_{tun} = -I_{tun0} W L e^{-V_f/V_{ox}} \tag{2.2}$$

where I_{tun0} is a pre-exponential constant, W and L are the width and length of the tunneling junction oxide respectively, V_f is a fit parameter that depends on the oxide thickness and V_{ox} is the potential across the tunneling oxide.

There are two currents produced by Hot-electron injection, the injection current (I_{inj}) flowing between the channel and floating gate and the well current (I_b) flowing between the channel and the well. Hot-Electron Injection is less understood than Fowler-Nordheim tunneling, and as a result, Rahimi et al. have developed equations describing the currents produced by this process using empirical fits. The injection current depends on the channel current, gate-to-drain potential and source to drain potential and is described by:



(a) (b)

Figure 2.8: a)V_{fg} vs time while injecting for $V_{sd} = 6V$. A change in V_{fg} is clearly visible after injection has been stopped and all terminals have been relaxed to operating potentials. b)V_{fg} vs time while tunneling for $V_{tun} = 14V$. A change in V_{fg} is clearly visible after tunneling has been stopped and all terminals have been relaxed to operating potentials.

$$I_{inj} = \alpha I_s e^{-\frac{\beta}{(V_{gd}+\delta)^2}+\lambda V_{sd}} \tag{2.3}$$

where I_s is the channel curent, V_{gd} is the gate-to-drain potential, V_{sd} is the source-to-drain potential and α, β, δ, and λ are fit parameters obtained from measured data.

The second current that is produced by Hot-Electron Injection is the current flowing from the channel to the well caused by a non-ideal transfer of electrons to the floating gate. This current depends on the channel current, source-to-gate potential, source-to-drain potential, and the threshold voltage of the device. Rahimi et al describe this as:

$$I_b = \eta I_s \left(\gamma V_{sd} - \kappa V_{sg} + V_t\right) e^{\frac{-\lambda}{\gamma V_{sd} - \kappa V_{sg} + V_t}} \tag{2.4}$$

where I_s is the channel current, V_{sd} is the source-to-drain potential, V_{sg} is the source-to-gate potential, V_t is the threshold voltage of the device and η, γ, κ, and λ are fit parameters calculated from measured data.

Similar to [10] and [7], a very large resistor is connected between the floating gate and a dependent voltage source to aid the simulator in finding a DC operating point. To keep current from leaking off the floating gate, a voltage-controlled voltage source is put between

this large resistor and ground and is set to follow the potential on the floating gate to ensure there is no voltage drop across the resistor.

This model is very effective when used for adaptive applications such as an autonulling amplifier; moreover, it is able to store charge on its floating node. The charge storage characteristics observed after injection and tunneling are shown in Figure 2.8. Although this model is very useful in adaptive circuits it is not without its flaws. This synaptic model presented by Rahimi et al. is unable to perform any DC analyses and does not account for the reduction in output resistance seen in floating-gate devices due to coupling from parasitic capacitances.

2.5.3 Pulse Model

The third major model type is a model developed to perform well in a pulse-based programming environment. Hasler et al. have developed a mathematical model for injection in [15] that uses monitored values for channel current, source-to-drain potential and charege on the floating gate. This model is described by the equation:

$$I_{inj} = I_{inj0}\left(\frac{I_s}{I_{th}}e^{\frac{-\kappa\Delta V_{fg}}{V_{inj}}}\right)e^{\frac{\Delta V_{ds}}{V_{inj}}} \tag{2.5}$$

where I_{inj0} is a pre-exponential current, I_s is the channel current, I_{th} is the channel current when the floating gate is biased at the threshold voltage, V_{fg} is the potential on the floating gate, V_{ds} is the drain-to-source potential and V_{inj} is a parameter which depends on the drain-to-channel potential.

This model is esentially an extension of the model developed by Rahimi et al.[8] discussed in Section 2.5.2, and Gray et al, in [9], have expanded on Hasler et al's mathematical model implementing it using Verilog-A to create a controlled current source between the drain and floating gate as seen in Figure 2.9. Gray uses a similar method to [10] and [8] to aid the simulator in DC convergence. A large valued resistor is placed between a voltage-controlled voltage source and the floating gate to allow for DC convergence to be achieved. The negative monitoring terminal of the voltage-controlled voltage source is connected to a node in the circuit that is to be held at a desired potential. The positive monitoring terminal of the

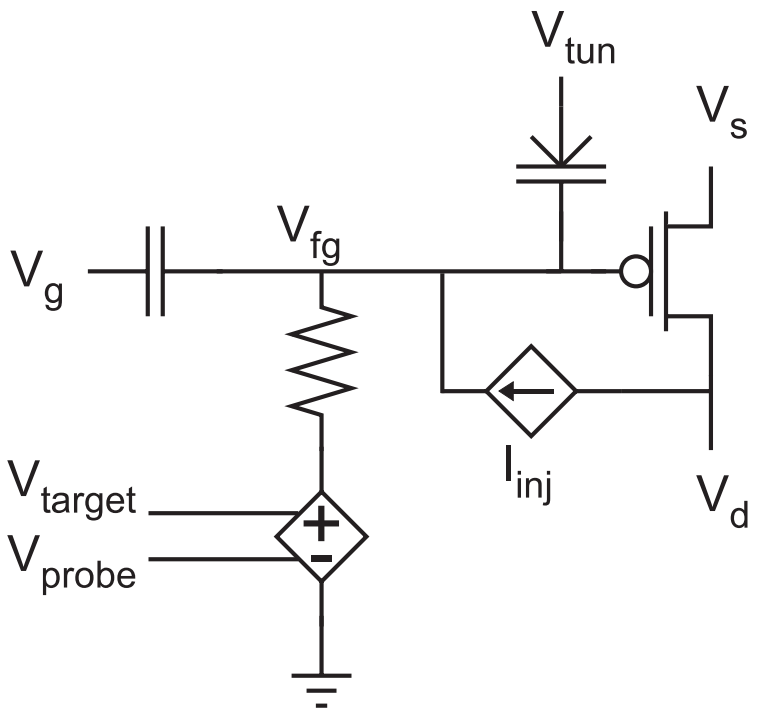


Figure 2.9: Schematic of the Floating-Gate MOSFET model proposed by Gray et al. in [9]. DC convergence is achieved in the same manner as in [10] and [8] by placing a large-valued resistor between the floating node and a DC voltage source configured such that no current flows through the resistor. This VCVS creates a negative feedback loop which sets the initial potential on the floating node. Hot-electron injection is modeled by a controlled current source implemented in Verilog-A using the mathematical model for injection proposed in [15].

voltage-controlled voltage source is connected to the desired potential. The voltage source then forces the floating node to a potential which allows a current to flow through the transistor which will maintain the desired potential.

While this model is able to converge on an initial DC operating point, it is unable to perform DC sweeps because the gate and tunneling potentials are coupling through capacitors which are seen as open circuits during DC simulations. Transient simulations are used to perform pseudo-DC gate sweeps to analyze the effective kappa as determined by the capacitive coupling of external potentials to the floating node. Figure 2.10 shows the effect of this coupling.

The primary focus of this model is performing hot-electron injection using changes in the various terminal voltages of the device during a time dependent analysis, and as such per-

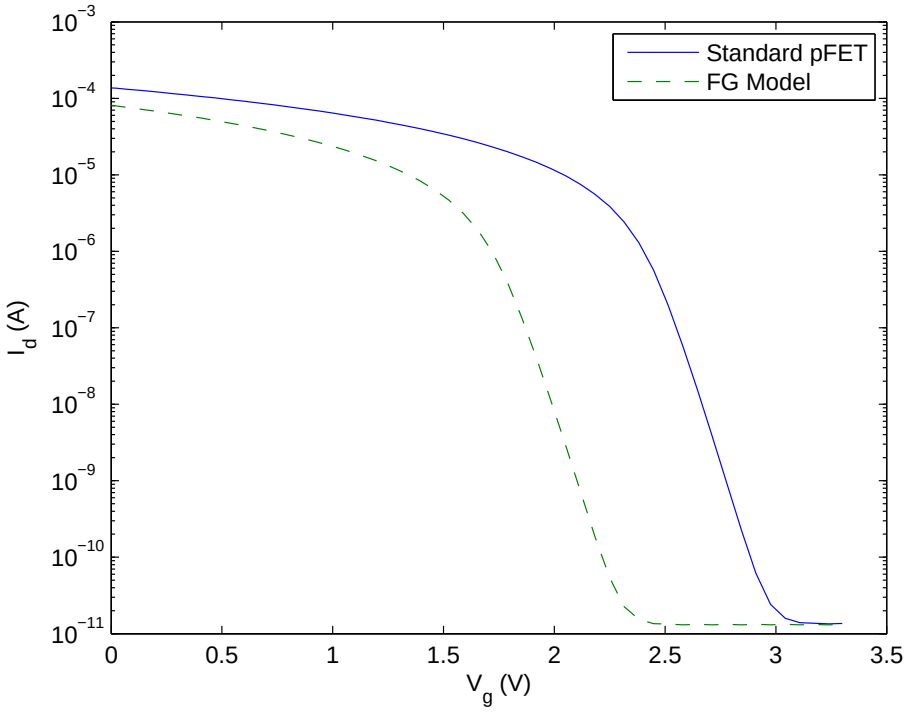


Figure 2.10: Gate sweep of a standard pFET (solid line) and the Floating-Gate model proposed by Gray et al (dashed line). The shallowing of the slope in the subthreshold region is a result of capacitive coupling of external potentials to the floating node.

forms well under these conditions. Figure 2.11 shows hot-electron injection being performed by pulsing the source-to-drain potential between V_{dd} and 6V.

As previously stated, this pulse-based model is very effective at modeling hot-electron injection when programming devices by pulsing the source-to-drain potential. The model also inherently models the coupling through the input capacitor and the coupling through the tunneling junction; however, this model does not model the coupling through the parasitic capacitors seen between the other terminals and the floating gate as seen in [10]. The modeling of this coupling through parasitic capacitors is only valid in transient simulations. Another inherent attribute being modeled here is the ability to store charge on the floating gate. This capability is displayed in Figure 2.11. Another major limitation of this model is the inability to perform any DC sweeps making characterization of DC performance especially difficult. This model works best when implemented in a pulse-based programming environment; however, the equations can also be applied to adaptive systems.

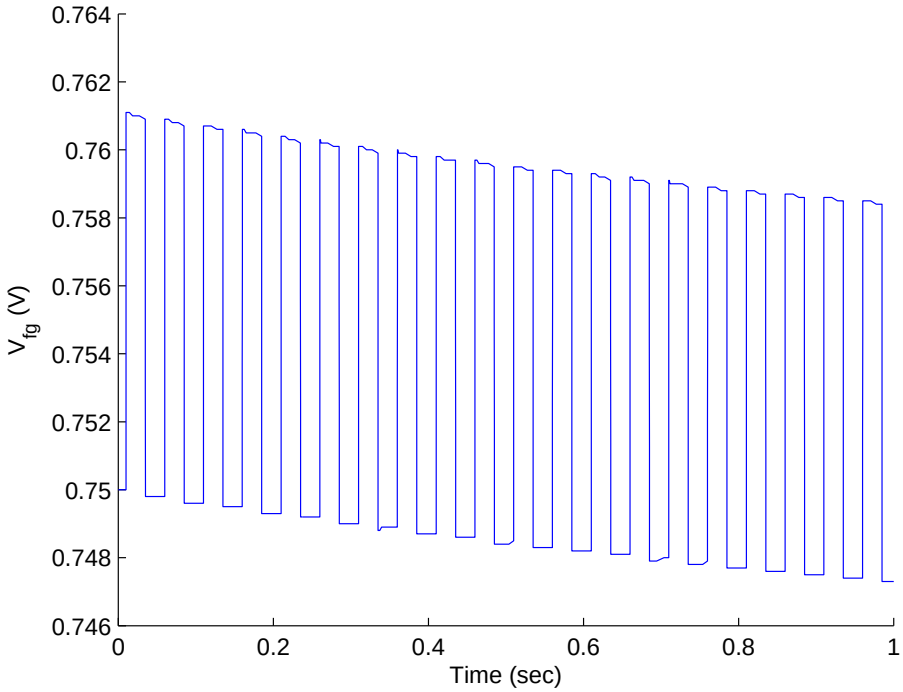


Figure 2.11: Model proposed by Gray et al performing injection during a series of pulses. V_{sd} is pulsed between 3.3V (normal voltage for a $0.5\mu m$ process) and 6V. A change in the charge on the floating gate is visible showing injection occuring as well as displaying charge storage capabilities of the model.

2.5.4 Summary

Each of the above models was designed to solve a specific problem with the simulation of floating-gate transistors, and they all perform reasonably under their designed conditions. Unfortunately, none of the existing models model every characteristic of floating-gate tre-ansistors; moreover, it would not be possible to modify any one of these models such that it would mimic every aspect of floating-gate transistors. Table 2.1 shows a summary of the capabilities of each of the models discussed in this Chapter. In the following Chapter, we will discuss the creation and operation of our new model which mimics all behaviors of floating-gate transistors.

	DC Analysis	Transient Analysis	Charge Storage	Hot-Electron Injection	Fowler-Nordheim Tunneling	Coupling Effects
Mondragon-Torrres et al.[7]	X	X				X
Sinencio Coupling [11]		X				X
Gray et al.[9]		X	X	X		
Rahimi et al.[8]		X	X	X	X	

Table 2.1: Summary of the capabilities of previous modeling attempts

Chapter 3

A New Model for Floating-Gate Transistors

As discussed in Section 2.5, several attempts have been made at modeling the characteristics of floating-gate transistors, with varying levels of success; however, no models to date have been able to duplicate all charateristics of floating-gate transistors. This chapter will cover the development of our proposed model which displays all characteristics of a physical floating-gate transistor; moreover, our model is platform-independent which allows it to be standardized across existing SPICE simulators. Section 3.1 describes the creation of a new circuit topology for modeling floating-gate transistors in standard SPICE simulators while Section 3.2 discusses the creation of the simulation model including modeling DC characteristics, hot-electron injection and Fowler-Nordheim tunneling.

3.1 A New Simulation Topology

One of the key developments we made was the creation of a new topology for allowing floating-gate transistors to be simulated using existing primitives within SPICE. The use of existing SPICE primitives allows for all types of analysis to be performed including DC operating point, transient, AC, etc. This represents a significant breakthrough in the modeling of floating-gate transistors as previous models are not as versatile.

The method developed here, shown in Figure 3.1, breaks a single floating-gate tran-

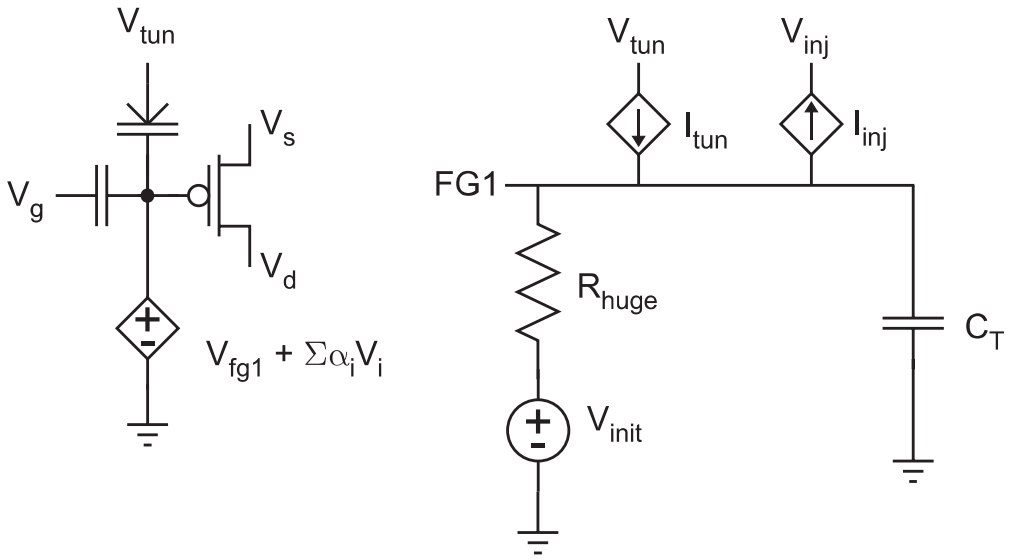


Figure 3.1: Structure of new floating-gate simulation model topology. In this structure a "dummy" node is used to compute the charge on the floating gate. This dummy node contains a very large resistor to ground (through a voltage source) that aids DC convergence but makes the node appear to be floating during simulation. The alpha terms represent coupling to the true floating gate node from each of the transistor's terminals through capacitive dividers (i.e. $\alpha_i = C_i/C_T$).

sistor into two nodes allowing for charge storage while maintaining valid current-voltage relationships for the device. The incorporation of this new topology into SPICE simulators is relatively simple and allows for easy access to foundry-supplied transistor models (i.e. BSIM3, EKV, PSP, etc) as well as foundry-provided parameters. The use of these models supplied by the various foundries yields the most accurate results when comparing simulations to data from fabricated circuits; moreover, the use of these foundry-supplied models does not require a lengthy characterization of transistors for each new process.

The principle concept of this new way of modeling floating-gate transistors revolves around creating an isolated "dummy" node for computing the appropriate amount of charge on the floating gate. This charge is mirrored to the actual floating gate via a voltage controlled voltage source. The exact voltage on the true floating gate is determined by a combination of the charge on the floating gate and also voltage coupling onto the floating gate through capacitors (both explicitly drawn and parasitic). The dummy node contains a voltage source that specifies the initial charge on the floating gate that connects to the

dummy node through a very large resistor (typically the maximum allowable resistance). This large resistor aids DC convergence of the simulator, but it looks like an open circuit in transient analyses so that charge is essentially held indefinitely on the floating node.

In addition to using voltage-controlled voltage sources to apply the proper amount of charge to the floating node, we use voltage-controlled current sources to alter the charge on the floating node. These voltage-controlled current sources are used to charge and discharge C_T (Figure 3.1), thus changing charge on the floating node. There are two voltage-controlled current sources in the model: one to model injection and one to model tunneling. The equations governing the operation of these current sources are derived from the works of Hasler et al. in [15] and Rahimi et al. in [8].

The actual floating gate voltage is set by adding the stored charge to a weighted average of all the other voltages coupling onto the floating node. This technique is essential for modeling the appropriate output resistance of floating-gate transistors, which tends to be much smaller than that of standard FETs due to feedback through parasitic capacitances as discussed in 2.2.

3.2 Creating the Simulation Model

As detailed in the previous chapter, the most fundamental attributes that must be modeled to properly design with floating-gate transistors are (1) the DC characteristics and small-signal AC parameters, (2) hot-electron injection for adding electrons to the floating node and (3) Fowler-Nordheim tunneling for removing electrons from the floating node. In the following subsections, we present the methods used to characterize these attributes as well as results from our simulation model.

3.2.1 DC Characteristics and AC Small-Signal Parameters

By characterizing various floating-gate test cells, which exposed the floating gate through an unity-gain-connected operational amplifier, it was possible to determine the coupling coefficients from all the terminals to the floating node. These coupling coefficients are represented as gain multipliers on the voltage-controlled voltage source connected to the floating node

of the transistor in figure 3.1 and are defined by

$$\alpha_x = \frac{C_x}{C_T} \tag{3.1}$$

where α_x is the coupling coefficient from terminal "x" to the floating node, C_x is the capacitance seen between terminal "x" and the floating node and C_T is the total capacitance connected to the floating node. Each of the α terms was found from the afforementioned floating-gate test cell which has all terminals "pinned-out" including the floating node which was connected through a unity-gain-connected operational amplifier allowing the voltage to monitored without having any effect on the floating gate voltage. These α terms were measured by sweeping each of the terminals of the device while holding the others at a constant potential and measuring the floating-node potential. The ratio of change in the floating-node potential to change in the swept terminal potential is the value of α_x (i.e. $\alpha_x = \frac{\Delta V_{fg}}{\Delta V_x}$). Table 3.1 shows the extracted values for the various coupling coefficients under the different regions of operation for a minimum-sized floating-gate transistor in a 0.5μm process.

	Subthreshold Ohmic	Subthreshold Saturation	Above Threshold Ohmic	Above Threshold Saturation
CG to FG	0.7987	0.8038	0.7945	0.7952
D to FG	0.0068	0.0037	0.0200	0.0003
Tun to FG	0.0047	0.0046	0.0044	0.0045

Table 3.1: Coupling Coefficients for Floating-Gate Transistor (0.5μm process)

Using the extracted parameters in Table 3.1, we compared the results of DC sweeps of our simulation model to the actual data from a fabricated floating-gate transistor, and found the model to follow real-world data very closely.

Figure 3.2(a) shows data taken from an actual floating-gate transistor. The control gate was swept and the channel current as well as the voltage on the floating node was measured, and the channel current was then plotted against the control gate potential and the floating gate potential. Plotting the channel current against the potential on the floating node allows us to observe the current-voltage relationship of the floating-gate transistor as though it were a standard MOSFET. Observing the subthreshold slopes of the two curves it can be seen

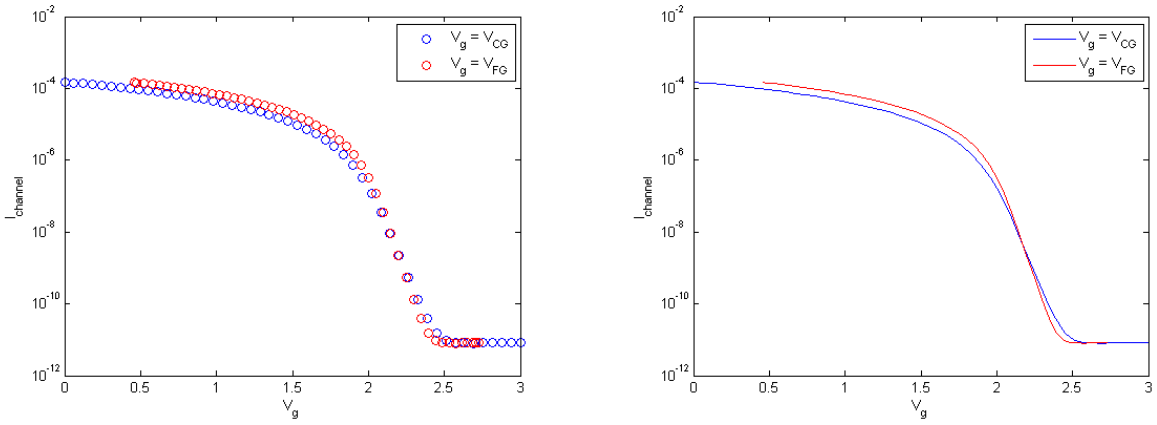


Figure 3.2: Gate sweep of a floating-gate transistor when sweeping the control gate. By observing the voltage on the floating-gate via a unity-gain buffer isolating that node, we are able to see the operation of the transistor itself (i.e. as though it were a standard MOSFET). As can be seen, the floating-gate transisotr has a smaller subthreshold slope than a standard transistor. Both slopes are characterized well by our floating-gate model. (a)Actual data from a fabricated floating-gate transistor. (b)Simulated data showing strong agreement with the real data.

that the slope of the floating-gate curve is smaller than that of the standard MOSFET. This difference is due to the capacitive division that occurs between the control gate and the floating gate. The subthreshold slope for a standard MOSFET can be described by $\frac{\kappa}{U_T}$ where κ is the coupling from the gate to the surface potential and U_T is the thermal voltage described by $\frac{kT}{q}$ and is approximately 25.9mV at room temperature. The subthreshold slope of a floating-gate transistor (when looking into the control gate) can be described by

$$\frac{\kappa_{eff}}{U_T} = \frac{C_g}{C_T}\frac{\kappa}{U_T} \tag{3.2}$$

where C_g is the capacitance between the floating gate and control gate and C_T is the total capacitance connected to the floating gate. As a result of this additional coupling term the subthreshold slope of a floating-gate transistor is reduced compared to a standard MOSFET. Figure 3.2(b) shows the results of the simulations performed using our model; these results closely follow those of a fabricated transistor, seen in Figure 3.2(a), showing a reduction in subthreshold slope.

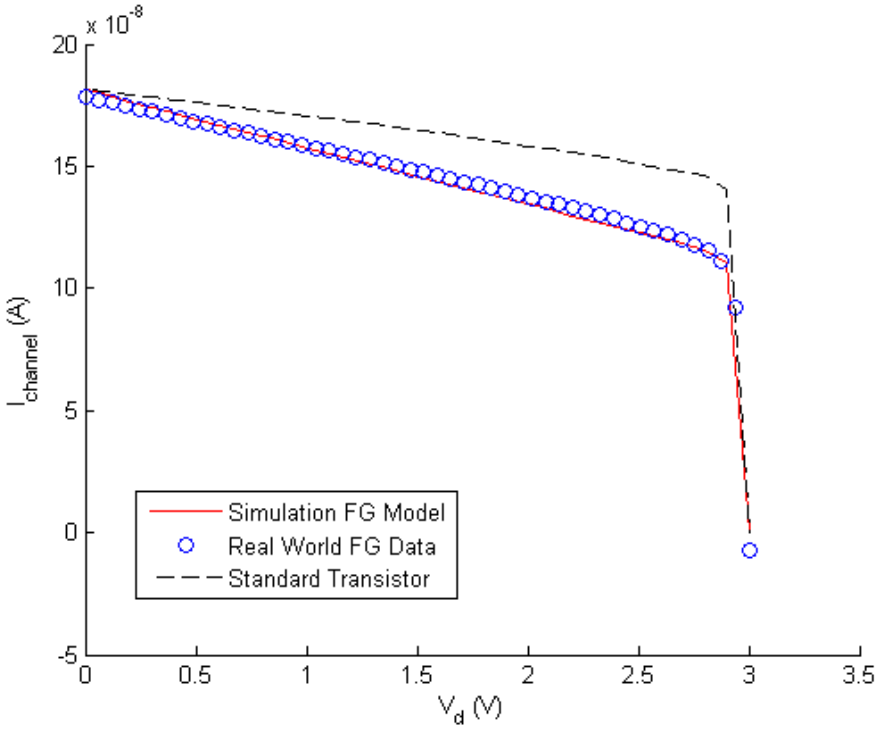


Figure 3.3: Drain sweeps of standard and floating-gate transistors. These data show that our simulation model closely models the drain characteristics of a floating-gate transistor. In this example, a subthreshold bias is shown and the simulated results (solid line) correctly follow the actual measured results from a fabricated floating-gate transistor (circles). To illustrate how the capacitive coupling effects significantly alter the performance of floating-gate transistor, the dashed line shows the results from a standard MOSFET transistor, which clearly has a much higher output resistance.

DC drain sweeps are another important method of charcterizing transistors because it allows us to determine the saturation and ohmic regions of operation as well as the output resistance of the device. Figure 3.3 shows a comparison of the results of a fabricated floating-gate transistor, our simulation model and a standard MOSFET; moreover, this figure shows that our model follows the output resistance of actual floating-gate devices very closely as well as the great variation in output resistance between standard MOSFETs and floating-gate devices.

3.2.2 Fowler-Nordheim Tunneling

For a complete model it is necessary to model the quantum mechanical processes involved in programming floating-gate devices. One of these proceses is Fowler-Nordheim tunneling and to properly model this process we characterized stand-alone tunneling junctions. The tested tunneling junctions were MOS varactors which are fabricated by placing a polysilicon gate over thin oxide and in close proximity to n+ type material within an n-well (assuming an n-well CMOS process). By sweeping the voltage across the junction, measuring the current through it and curve-fitting this data we found the current-voltage relationship of this device to be

$$I_{tun} = I_{tun0} e^{\frac{-V_{tun0}}{V_{tun} - V_{fg}}} \tag{3.3}$$

where I_{tun0} and V_{tun0} are curve fit parameters, V_{fg} is the floating gate voltage and V_{tun} is the potential on the other side of the junction.

Figure 3.4 shows the results of these sweeps and the corresponding curve-fit from which equation (3.3) is derived. This equation governs the current supplied by the I_{tun} voltage controlled current source in Figure 3.1. We were only able to reliably measure tunneling currents over 2.5 decades of current due to device and equipment limitations. We were restricted by the current-measurement limitations of our picoammeter on the low-end, and on the high-end we were limited by the maximum allowable voltage across the device without damaging it (17.5V). However, these data provide sufficient information to obtain a good characterization and can be extrapolated for lower current levels.

As a demonstration of the simulation model working properly, we devised an experiment in which we pulsed the tunneling junction with a sufficiently high voltage to induce tunneling for 1ms. Between each pulse, a DC gate sweep was performed to show that the charge stored on the floating gate has moved. To start the experiment, an initial gate sweep was performed to record a starting point (black curve); the tunneling voltage was then raised to a large potential ($\tilde{1}$5V) for 1ms and reduced to an operating potential ($V_{dd} = 3.3V$). A DC gate sweep was then performed to record the effect of the tunneling current. This process was repeated several times. Figure 3.5 shows the results of this experiment. As can be seen in

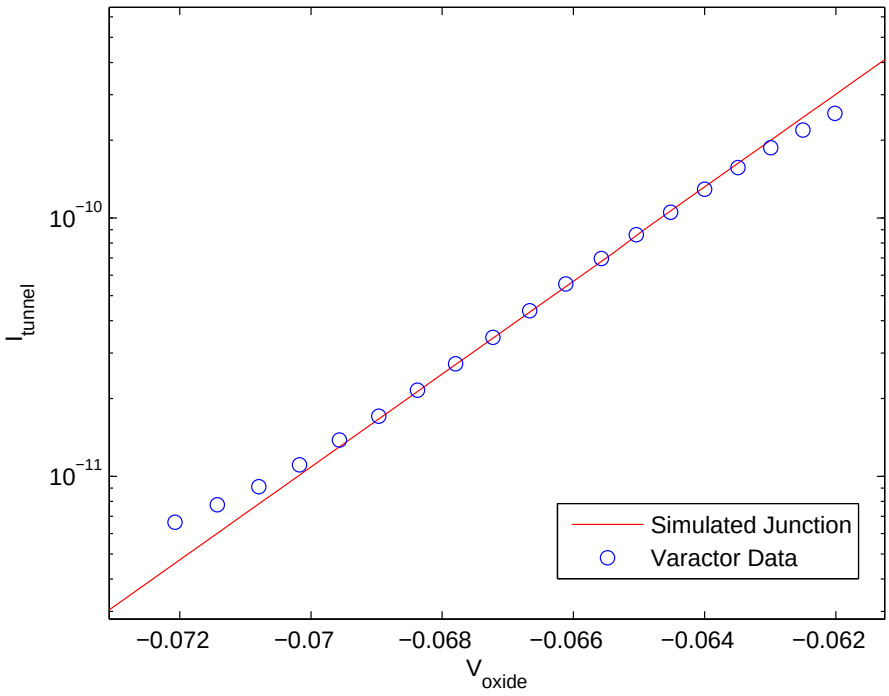


Figure 3.4: Characterization and simulation results of Fowler-Nordheim tunneling. Data (circles) from I-V sweeps of an isolated tunneling junction are curve fitted to obtain an I-V relationship that can be implemented in SPICE. The SPICE simulation results (solid line) clearly agree with the actual values of current.

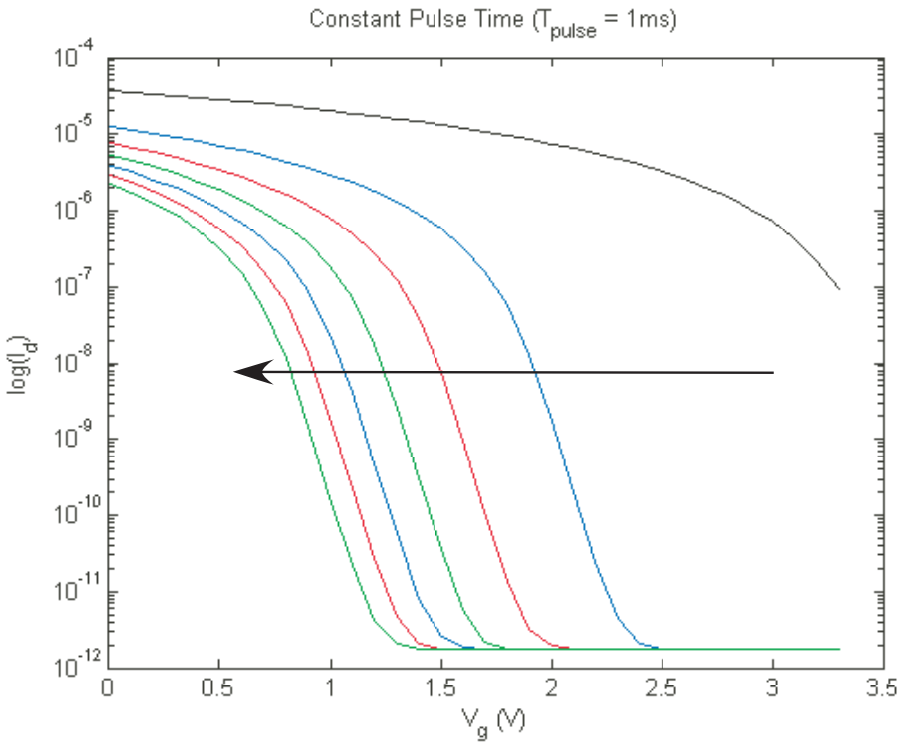


Figure 3.5: Results of tunneling a floating-gate transistor. A large tunneling voltage is applied for 1ms several times. After each pulse the current is measured using a DC gate sweep to show that the charge has been modified. Each tunneling pulse moves the curve to the left. While all pulses are uniform, the actual voltage on the floating gate is increasing and as such the potential difference across the tunneling junction is decreased reducing the current through the junction with each iteration.

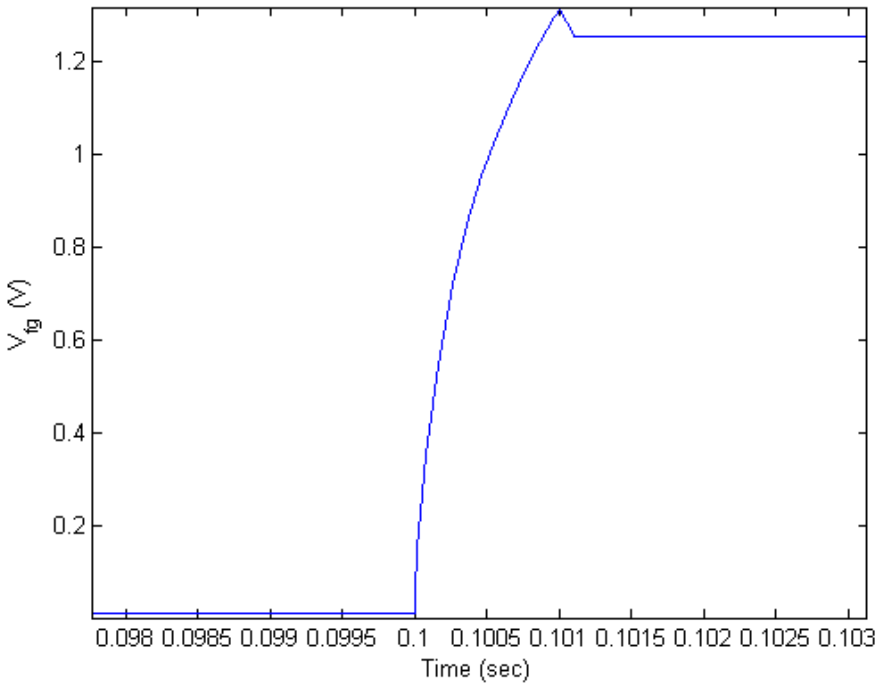


Figure 3.6: Transient simulation results of our floating-gate transistor model incorporating Fowler-Nordheim tunneling. A large tunneling voltage is applied from 0.1 to 0.101s, and during this time interval the floating gate voltage increases. At all other times, the tunneling voltage is small and there is no tunneling; therefore, the floating gate voltage remains constant.

this figure, each time a large tunneling potential is applied the threshold voltage is shifted farther from V_{dd}. It can also be observed that tunneling is a self-limiting process due to the fact that I_{tun} is a function of $V_{tun} - V_{fg}$; since V_{fg} increases with each iteration, this difference decreases and the tunneling current decreases as a result.

Figure 3.6 shows the simulated effects of Fowler-Nordheim tunneling on the floating gate voltage. A large potential is applied to the tunneling junction starting at 0.1 seconds and returned to a normal operating potential at 0.101 seconds. During this time, when tunneling is active (i.e. $V_{tun} > V_{dd}$), the floating-gate voltage increases, and after the tunneling voltage returns to normal operating potentials ($V_{tun} \leq V_{dd}$), it can be seen that the change in charge is stored on the floating gate. The effects of capacitive coupling can also be observed. At the time that tunneling is stopped (0.101s) a small reduction in the floating-gate potential

can been seen; this is due to the capacitive coupling from the tunneling voltage through the tunneling junction (i.e. the α_{tun} term in table 3.1).

3.2.3 Hot-Electron Injection

Modeling hot-electron injection is much more complicated than modeling tunneling because injection depends on several parameters including the channel current, source-to-drain potential and the gate-to-drain potential. Additionally, these relationships are all non-linear in nature. Furthermore, there is no way to directly observe injection current; it can only be observed indirectly by monitoring what it affects. To determine the injection current, we performed the following test. We set the current flowing through the floating-gate transistor to be a small current on the order of 10nA and we placed a large voltage between the source and drain (i.e. $V_{sd} > V_{dd}$) and as a result, injection is "turned on." We measured the starting current through the channel and the change in current after some specified amount of time ΔT. We repeated this experiment for varying values of V_{sd}. The results of this experiment are shown in Figure 3.8, and these results allow us to determine the injection current.

The injection current, I_{inj}, can be found by understanding that I_{inj} modifies the charge on the floating gate, and the floating gate voltage establishes the amount of current flowing through the channel. We can then calculate the actual injection current by using the following relationship

$$I_{inj} = -\frac{C_T}{T}\frac{I_s}{g_m}\frac{\Delta I_s}{I_s} \tag{3.4}$$

where C_T is the total capacitance connected to the floating gate, T is the time between each measurement, g_m is the transconductance of the floating gate transistor, I_s is the channel current and ΔI_s is the change in channel current resulting from injection during each time interval. By using this methodology, we obtain the injection currents for a given I_s and V_{sd} as shown in Figure 3.7.

It is also possible to determine the injection current by monitoring the floating-gate voltage. To do this, we connect a unity-gain-connected operational amplifier to the floating node. This buffer circuit allows us to monitor the floating-gate voltage without having any

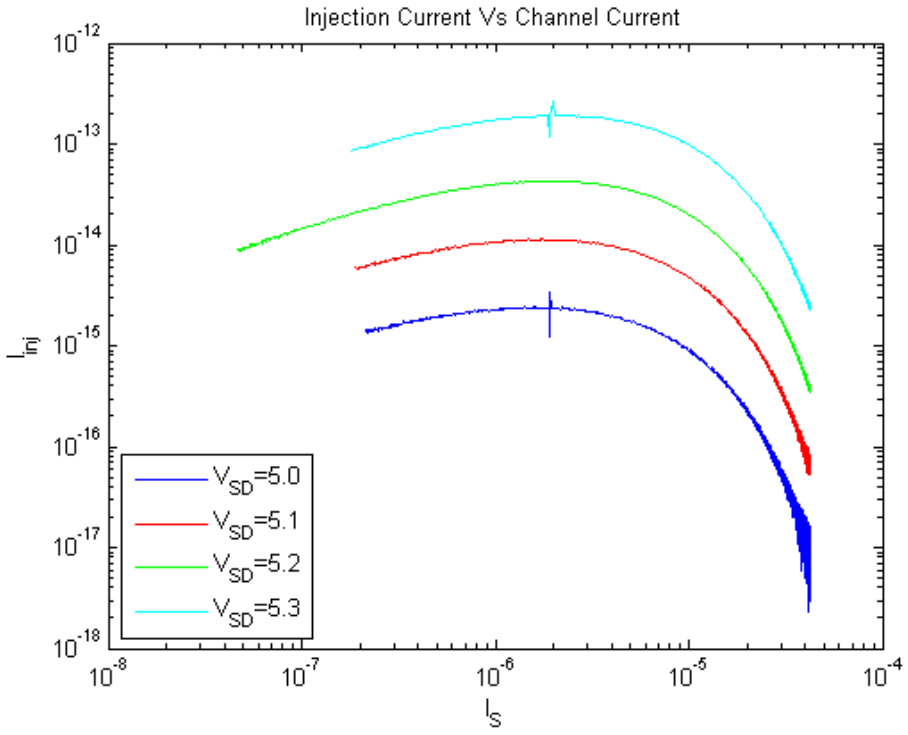


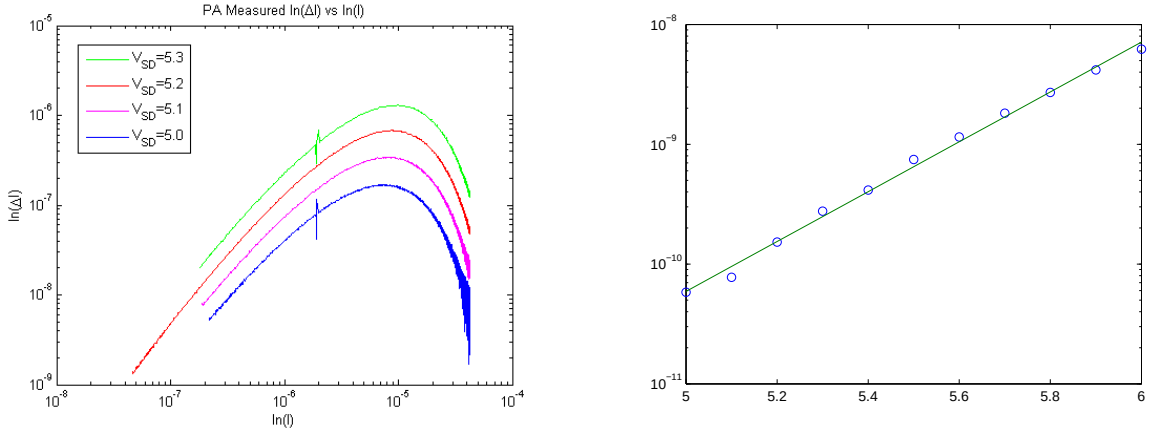
Figure 3.7: I_inj vs I_s for a floating-gate transistor fabricated on a 0.5μm CMOS process. I_inj is calculated using equation 3.4 because the injection current is not directly measurable.

effect on the potential. Knowing the floating-gate voltage and the total capacitance on the floating-gate, we can calculate the injection current using the current-voltage relationship

$$I_{inj} = C_T \frac{dV_{fg}}{dt} \tag{3.5}$$

where C_T is the total capcitance connected to the floating gate, dV_{fg} is the change in floating-gate voltage, and dt is the time each injection pulse. Using this setup, we ran the same test as in the first method of determining injection current. Figure 3.7b shows the injection current calculated using equation 3.5 vs channel current.

The data shown in Figure 3.8 can be used to determine an injection model. The compact models presented in [8][9][15][16] were investigated and we found the injection model presented by Huang et al in [16] to be the most effective and easiest to demonstrate. It should be noted that the model demonstrated here is only valid for subthreshold current levels; however, because of the modular design of this model any mathematical model for injection



(a) (b)

Figure 3.8: (a)ΔI_s vs I_s for a floating-gate transistor fabricated on a 0.5μm CMOS process. The channel current for a particular V_{gate} and V_{sd} is measured. The device is then injected for some specified amount of time, and then the channel current is measured again to obtain the resulting change in channel current, ΔI_s. (b)I_{inj} vs V_{sd}. This plot is generated by selecting a single value for channel current, I_s, and "picking off" the value of I_{inj} for each value of V_{sd}. The circles represent these values of I_{inj} and the line is the polynomial fit. The slope of this polynomial fit is $1/Vinj$

can be easily used. The following equation, developed by Huang et al.[17][16], governs the I_{inj} voltage-controlled current source in Figure 3.1.

$$I_{inj} = \alpha I_s e^{\frac{V_s - V_d}{V_{inj}}} \tag{3.6}$$

The fit constants α, and V_{inj} are determined by curve-fitting the data in Figure 3.8. The effect of the source-to-drain potential can be determined from the following analysis. We choose some subthreshold current from Figure 3.8 and "pick off" the values of I_{inj} for each V_{sd} value. These values of I_{inj} are then plotted versus the values of V_{sd} used and the slope of the resulting curve is $1/V_{inj}$ which defines the V_{sd} dependency. This process is illustrated in Figure 3.8(b). The α fit constant in equation 3.6 is found by using the value of V_{inj}, determined above, and solving equation 3.6 for α. Using the values of these fit contants, we are able to predict a proper injection current for subthreshold channel currents. The results of this fit can be seen in Figure 3.9.

To verify that our complete injection model was working, we ran two different exper-

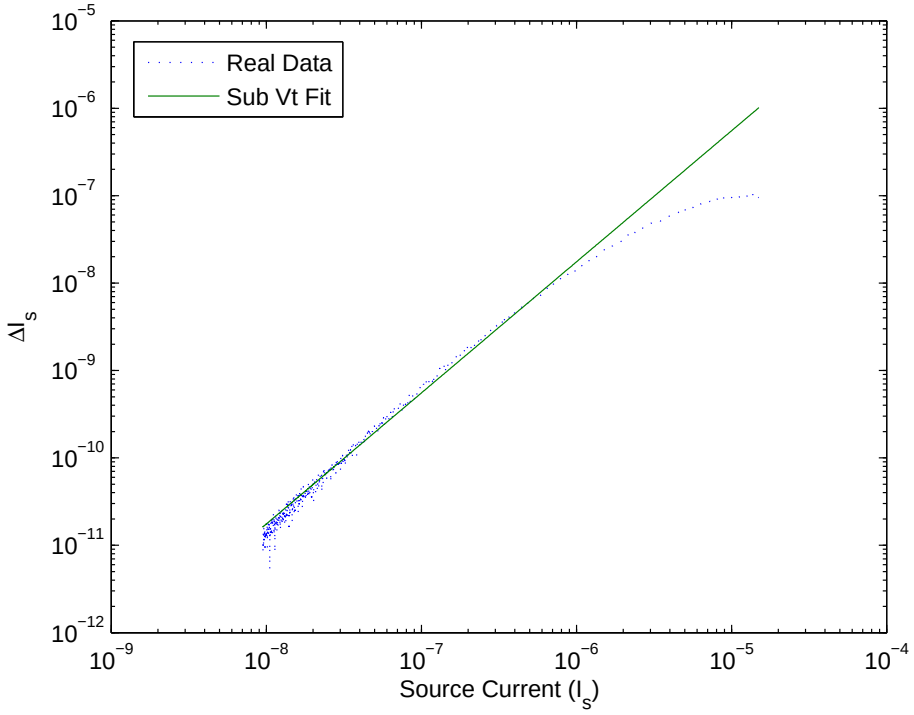
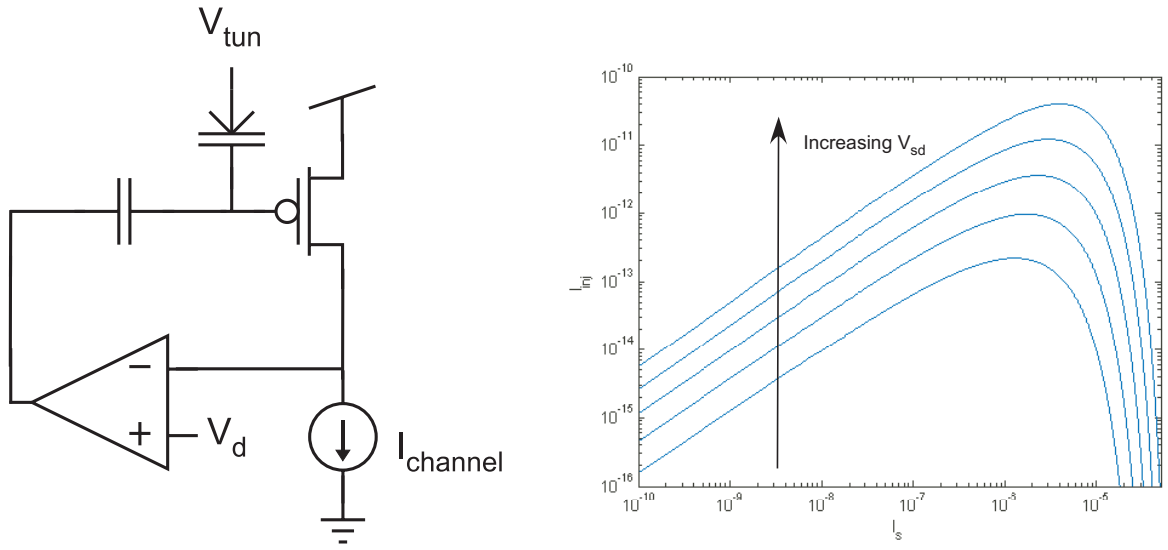


Figure 3.9: Change in channel current vs channel current for a floating-gate transistor fabricated on a 0.5μm CMOS process. The dotted line represents data take from a real floating-gate transistor while the solid line represents values calculated from equation 3.6.

iments. The first experiment was run using the setup shown in Figure 3.10(a). In this configuration, the channel current, I_s, is swept while V_{sd} is held constant. This injection current is measured, and the resulting simulated injection current is shown in Figure 3.10(b) for various values of V_{sd}.

The second experiment was a series of injection pulses which allowed us to verify the charge storage aspect of the modeled floating-gate transistor when performing hot-electron injection. In this experiment, we defined a length of time over which injection would occur. We also explicitly set the V_{sd} at which injection would occur; moreover, we held these values constant throughout the experiment. As shown in Figure 3.11, the source potential is connected to a high potential and the drain potential was pulsed from some high potential down to a low potential, such that $V_{sd} > V_{dd}$ during the 1ms pulse. A gate sweep was taken before any injection occurred as well as after each injection pulse. The control gate was held constant throughout the experiment. Figure 3.12(a) shows the results of this experiment, and



(a) (b)

Figure 3.10: (a)Schematic of the test setup for gathering I_{inj} vs I_s simulation data. The operational amplifier forces the drain to stay constant at voltage V_d because of negative feedback. The channel current is swept, causing injection to occur at different rates. (b)Simulated I_{inj} vs I_s using the test setup shown in (a). Each curve represents the results for a different value of V_{sd}, increasing from bottom to top.

in this figure we can see the channel current increased with each pulse. Figure 3.12(b) shows the transient response of the floating gate for one of these injection pulses; in this case, the charge on the floating gate is only modified while injection is occurring (i.e. $V_{sd} > V_{dd}$). The floating gate voltage remains constant while $V_{sd} \leq V_{dd}$; moreover, similar to the tunneling transient response in Figure 3.6, we can see the effect of capacitive coupling onto the floating gate.

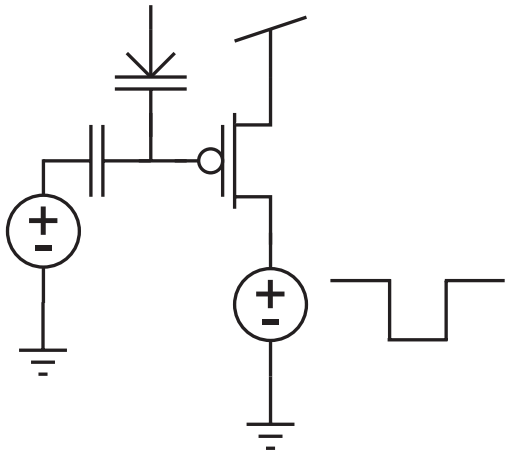
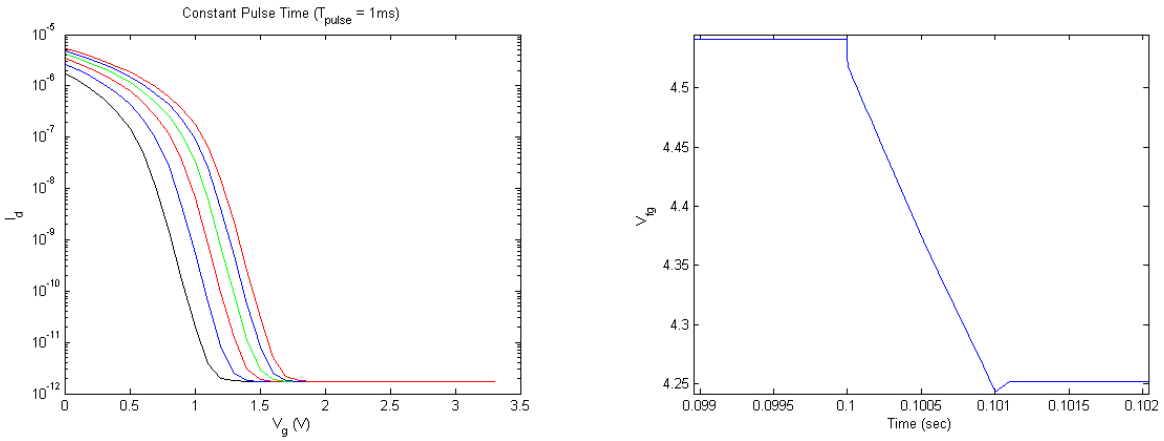


Figure 3.11: Schematic of the setup for injection pulsing experiment. The source of the transistor is held at a high potential and the drain is pulsed to a lower potential such that $V_{sd} > V_{dd}$.



(a) (b)

Figure 3.12: (a)Simulated gate sweeps of our floating-gate model following a series of hot-electron injection pulses. Each curve was taken after a pulse of 1ms at a V_{sd} of 6V. This particular result shows the case of a floating-gate transistor starting with a current that is slightly above the threshold current; therefore, each interation causes less electrons to be injected onto the floating gate. (b)Transient simulation results of our floating-gate transistor model incorporating hot-electron injection. An injection current is applied by pulsing the drain voltage down from some high potential to a much lower potential such that $V_{sd} > V_{dd}$ during the injection pulse. The injection pulse is applied from 0.1s to 0.101s (1ms), and during this time interval, the floating gate voltage decreases. At all other times, V_{sd} is small and injection does not occur; therefore, the floating gate voltage remains constant.

Chapter 4

Application of the Model

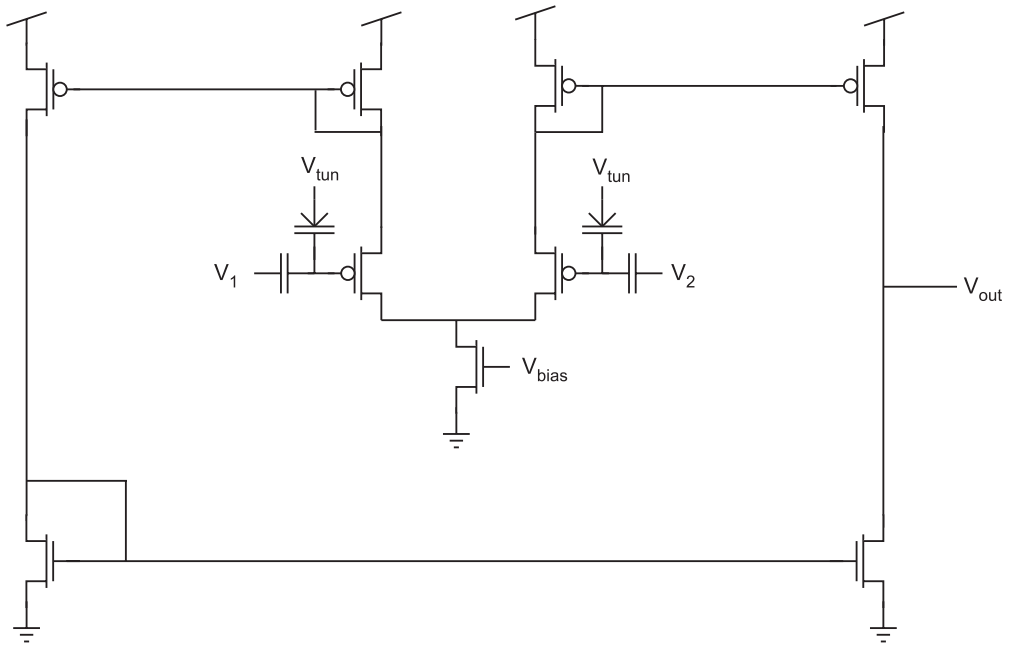


Figure 4.1: Schematic of a standard 9-transistor OTA using floating-gate transistors for inputs to the amplifier.

In Chapter 3 we discussed the development of the new model and in this chapter we will demonstrate the model simulating three uses of floating-gate transistors: (1) removing offset due to device mismatch in an operational transconductance amplifier (OTA), (2) increasing the linear range of an OTA using capacitive division at the input transistors, and (3) using hot electron injection to program a floating-gate device to a target level.

4.1 Offset Correction

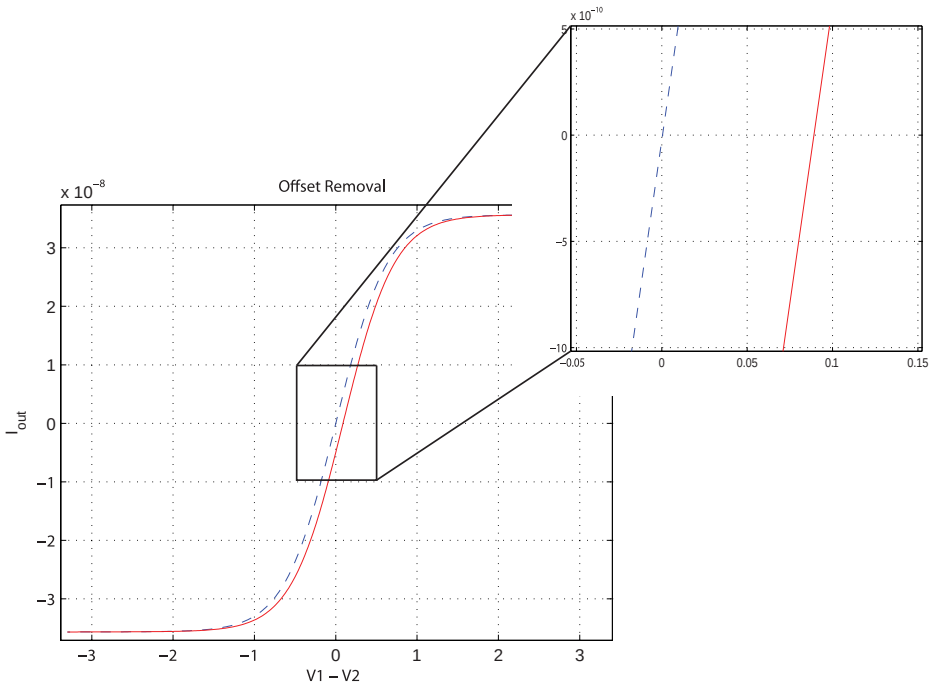


Figure 4.2: Nine-transistor OTA with floating-gate differential inputs. The solid line shows offset due to device mismatch while the dashed line shows this offset being corrected by altering the charge on the floating-gates.

As discussed in Chapter 1, device mismatch is a significant problem that must be overcome by analog designers. Differential circuits, such as OTAs, are particularly sensitive to mismatch because their operation is dependent on the fabrication of identical devices. A standard nine-transistor OTA has four pairs of transistors: the input transistors and 3 current mirrors [18]. Each of these pairs needs to be identical such that the gain of each current mirror is 1 and the same amount of current flows through each of the input transistors when $V_+ = V-$. If any of these pairs do not contain identical devices, an offset will be introduced to the system. This offset can be removed by using floating-gate transistors [19] for the input pair, as seen in Figure 4.1, and programming each floating node with an appropriate charge such that the V-I characteristics of each half of the system are identical. Simulation results of this offset removal are shown in figure 4.2. As can be seen, our floating-gate simulation model can be programmed such that this offset is removed.

4.2 Multiple Input Floating-Gates

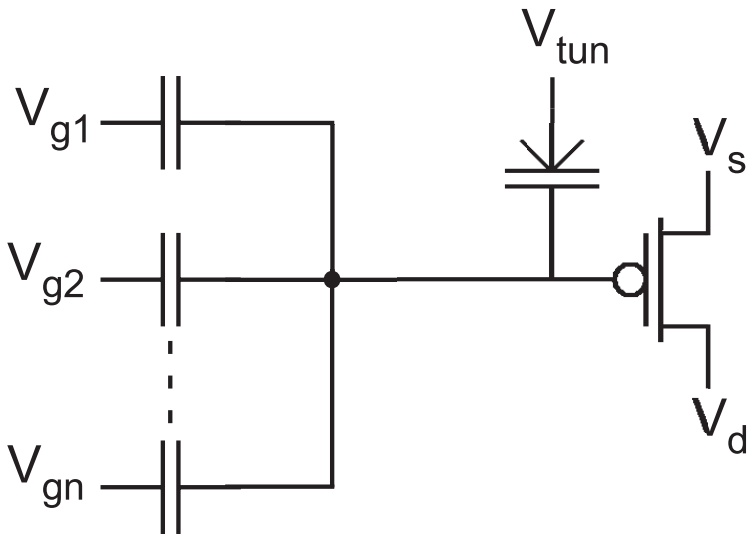


Figure 4.3: Schematic representation of a Multiple-Input Floating-Gate Transistor. Each input is coupled to the floating node through an independent capacitor.

Multiple input floating-gate (MIFG) transistors are, simply, floating-gate transistors with multiple control gates, each coupling to the floating node through a separate capacitor. A schematic representation of a MIFG device is shown in Figure 4.3. The model presented in Chapter 3 is easily modified to accomodate multiple inputs to the floating node by making the following changes: (1) Add the values of the additional input capacitors to the total capacitance on the floating gate, C_T and (2) Add an additional VCVS to the floating node to represent the coupling through the additional capacitor.

We can use MIFG transistors to add capacitive division to the input terminals of an OTA. Capacitive dividers on the inputs of an OTA alter the linear range of the device and has been shown as a successful method of increasing the linear range. By dividing down the applied voltages on the input of the OTA we reduce the range of potentials seen by the differential inputs, thus causing a larger range of applied potentials to be within the linear range of the device [20]. Figure 4.4 shows the change in linear range caused by altering the capacitive division ratio; as we reduce the ratio, the linear range is increased.

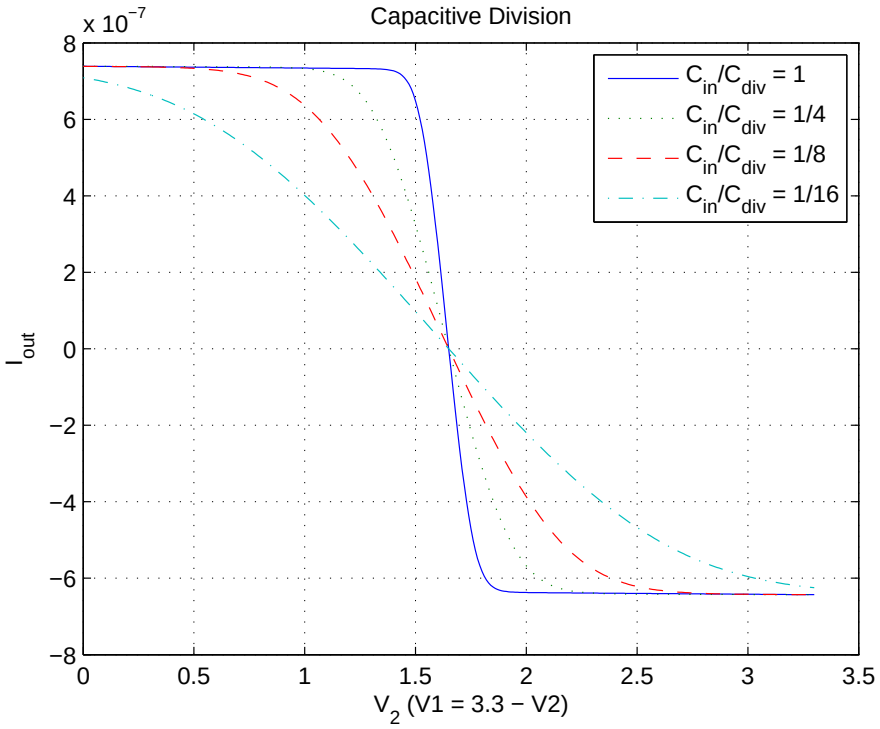


Figure 4.4: Comparison of different input capacitor ratios on a nine-transistor OTA with MIFGs used for the input pair. The reduction of the capacitor ratio increases the linear range of the device.

4.3 Floating-Gate Programming

In order to properly correct for offsets and mismatches in circuits, it must be possible to precisely program floating-gate devices to specific levels. One of the methods used to program floating-gate transistors is the pulsing method used by Hasler et al.[15]. In this method, we raise the potentials of each terminal by some amount. Once the potentials have been raised, the drain is pulsed to a lower potential such that the drain-to-source potential is sufficiently large enough to allow injection to occur at the desired rate.

To test the accuracy of our model we devised the following experiment based on the pule method of injection. First, a fabricated floating-gate transistor is injected to a desired target using a series of drain pulses; moreover, the amplitude of the drain pulses is reduced as the channel current approaches the target to prevent overshoot. Once the floating-gate transistor is programmed to the target current, the simulation model is programmed with the same

pulses used to program the floating-gate. Figure 4.5 shows the results of this experiment.

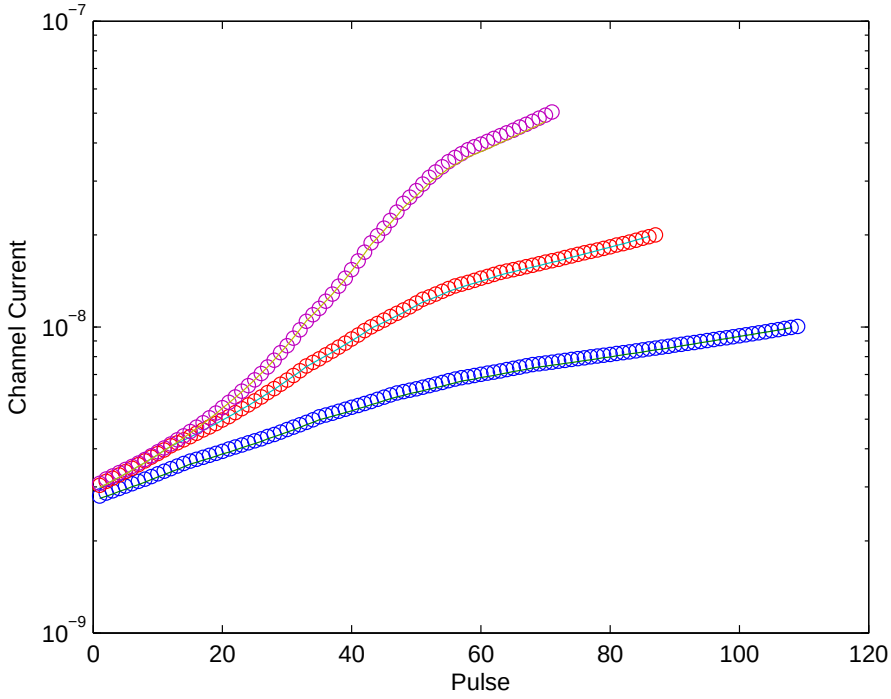


Figure 4.5: Channel current vs pulse number for three different target currents, 10nA, 20nA and 50nA. The circles show data taken from a floating-gate transistor fabricated on a 0.5μm process and the solid lines show the corresponding data taken using our simualtion model. Each pulse is 1ms in length and the source-to-drain potential varies from 6.5V to 5.9V.

Chapter 5

Conclusions and Future Work

In this work, we have developed a new way of approaching the simulation of floating-gate devices. This new method handles every type of simulation, including DC analysis, AC/small-signal analysis and transient analysis, and is also highly modular. The modular design allows for the SPICE primitives modeling hot-electron injection and Fowler-Nordheim tunneling to be altered as further developments are made in characterizing these processes. The use of SPICE primitives allows the model to be used with any existing simulator, including industry standards such as HSPICE and Cadence Spectre, with minimal effort required to port code.

This work provides a solid foundation on which to build further enhancements. For example, the hot-electron injection model used in this work is valid only in the subthreshold region of operation and further characterization is required to implement a valid model for all regions of operation. We have begun developing a model of hot-electron injection based on black body radiation. We are also currently working to port our model to Cadence Spectre which will offer a more integrated experience for integrated circuit design.

Appendix A

Further Considerations for Previous Models

A.1 Coupling Model

Considering the model presented by Yin et al.[10] in Figure 2.4, it is necessary that the input resistor, R_{in}, be orders of magnitude smaller than R_{gd}, R_{gs}, and R_{gw} to avoid a resistive divider of significant gain being formed in the DC case. If a resistive divider of sufficiently large gain is formed, the range of voltages the floating gate can assume for a given range of voltages applied to the control gate is compressed. The worst case scenario for this issue is all resistors connected to the floating gate are equal, and analyzing this case:

For $V_{cg} = V_d = 0V$ the overall gain of the resistive divider is:

$$\frac{V_{out}}{V_{in}} = \frac{R_{in}||R_{gd}}{(R_{gs}||R_{gw}) + (R_{in}||R_{gd})} = 0.5 \tag{A.1}$$

In this case we have assumed that the well and source are tied to V_{dd} and the control gate and drain are tied to ground. This sets the lower limit of V_{fg} which will be $0.5 * V_{dd}$ (1.65V in the case of a $0.5\mu m$ process).

To find the upper limit of V_{fg} we assume that $V_{cg} = V_{dd}$. We assume that the source and well are still tied to V_{dd} and the drain remains at ground. The gain of the resistive divider, in this case, becomes:

$$\frac{V_{out}}{V_{in}} = \frac{R_{gd}}{(R_{in}||R_{gs}||R_{gw}) + R_d} = 0.7502 \tag{A.2}$$

From this equation we determine the upper limit of V_{fg} to be $0.7502 * V_{dd}$ (2.476 in the case of a $0.5\mu m$ process). Figure A.1 shows the compression of the floating-gate voltage explained by equations (A.1) - (A.2).displays DC gate sweeps for a standard p-type MOSFET, the coupling model with matching time constants and the coupling model with equvialent resistors connected to the floating gate.

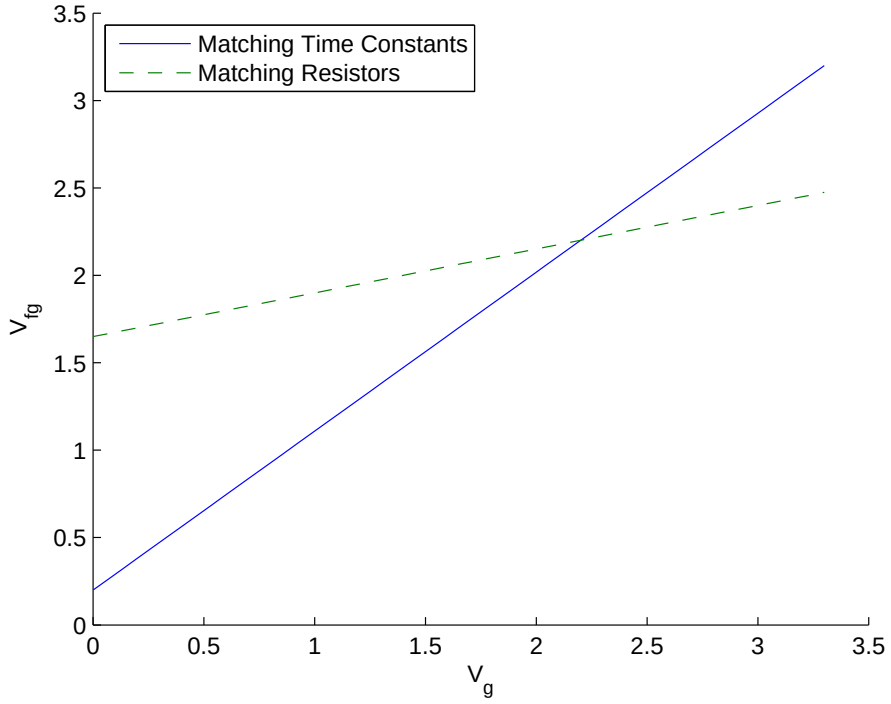


Figure A.1: Floating-gate voltage vs voltage applied to the control gate for the coupling model in [10] when all resistors connected to the floating node are equal (dashed line) and when all RC products connected to the floating node are equal (solid line). The compression of V_{fg} caused by the voltage divider formed on the floating node is very evident in the case where all resistors are equal.

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